Steven Mu

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Skills

Languages & Build Systems: C (User and Kernel space), C++, ARMv8 ISA, System Verilog, Python, Bash, Make, Meson
Tools & Environments: UNIX CLI, Linux, Embedded Linux, FreeRTOS, GDB, GCC, Git, Docker, Protocol Buffers, ZeroMQ, SQLite
Standards & Protocols: Scrum/Agile (Jira & Confluence), Jenkins CI/CD, MISRA C, JTAG Debuggers, CAN, UART, I2C, SPI
Other Skills: Altium, AMD Vivado, PCB Fab, Circuits, Datasheets, Oscilloscopes, OnShape, Wireshark

Experience

Embedded Software Engineering Intern – **Kepler Communications** Toronto, ON, Canada May 2025 – Current

- Flight Software team, developed embedded solutions for satellite fleet, to bring high-speed connectivity to space (Launch Jan 2026)
- Worked with **C and C++** for a very resource-constrained and timing-critical **AMD Zynq** SoC (**ARM Cortext-A53**, **Cortex-R5F, FPGA**)
- Led design & development of a **C++** embedded config app w/ **Protobuf** & **SQLIte3**. Wrote 90%+ coverage unit tests w/ **Google Test**
- Optimized an embedded service messaging system with a **ZeroMQ** based publish-subscribe bus. Used **GDB** extensively for debug.

Firmware Engineering Intern – **Ford Motor Company** Ottawa, ON, Canada Sep 2024 – Dec 2024

- Bootloader, BSP & Kernel team, developed drivers with **C in User & Kernel space** for **ARM Cortex-A53** SoC w/ resource-constraints
- Improved bootloader stability, reducing boot fails caused by **LPDDR Memory, eMMC, and Interrupt Controller (GIC-500)** to **0%**
- Optimized **Embedded Linux Kernel** by improving the suspend & resume sequence, added detailed callstack dumps in kernel panic
- Worked extensively with debug hardware (**Lauterbach PowerDebug JTAG + Trace32**). Managed work with Jira and Confluence

Embedded Software Intern – **450 Solutions** Tokyo, Japan Jan 2024 – Apr 2024

- Led a team of 4 interns on the design & development of an embedded system for a smart POS system, built for restaurants
- Worked with **C and C++** to develop drivers for a **Bluetooth LE** printer system. Also worked on optimizing power usage by interfacing with **display drivers** and the onboard **PMIC**. Improved end-to-end system speed by **25%** and reduced display power usage by **15%**

Interfacing Team Co-Lead – **WATONOMOUS** Waterloo, ON, Canada Jan 2024 – Dec 2024

- Co-led the development of vehicle embedded systems. Developed **sensor software** in **C** to collect & send metrics to an **info system**
- Worked with **Altium** to design & fabricate PCBs, including the distance sensor **controller** and its **Power** & **Communication** boards
- Wrote various **test fixtures in C++** using **Google Test**, also performed extensive constructive code reviews for other developers

Projects

Bare-Metal Bootloader & RTOS (SprinterOS) (Click to Learn More) Dec 2024 - Present

- High-performance **bare-metal** board bring up for an **ARM Cortex-M7** based STM32F767ZI board, without HAL or any libraries
- **Bootloader and Kernel** done using **C** and **ARMv7 Assembly,** with higher level software such as user CLI done in **C++**
- Completed **bootloader** Power Manager, RCC (clock controller), UART, NVIC (interrupt controller) drivers. Working on
- Completed **kernel** features like Context Switching, Dynamic Memory Allocation and a FCFS Scheduler w/ priority-based-preemption
- Used debug hardware (**SEGGER J-Link JTAG & STLink**) and **GDB CLI** to perform memory and register level debugging & verification

HDMI Graphics Unit w/ FPGA (Horizon Project) (Click to Learn More) July 2024 - Present

- HDMI graphics unit using a **Xilinx Spartan-7 XC7S50** based Digilent Arty S750 FPGA. Used to drive video output of SprinterOS CLI
- Completed system design stage, implemented a pixel clock generator using **MMCM**. Working on a pipelined video timing controller
- Interfaced with STM32F767ZI of SprinterOS with **QSPI.** Implementing and simulating using **System Verilog** in **AMD Vivado**

4-Bit Binary Adder Project w/ BJTs (Click to Learn More) Mar 2024 – Apr 2024

- Developed a 4-bit hardware binary adder with **transistor level** logic gates, with **SMD components**. Working on expansion to **full ALU.**
- Used **Altium** for circuit design & layout. Some PCBs etched myself, others manufactured. Debugged with **oscilloscope & multimeter**

Education

University of Waterloo – BAsc. - **Computer Engineering** Waterloo, ON, Canada Junior (3rd year)

- UWaterloo Varsity Men's Track and Field, ECE Wellness & Athletics Representative, UW Athletics & Recreation Student Leader
- **Awards:** USPORTS Academic All-Canadian (80%+ avg. as student athlete), B.P Dammizio Scholarship, President's Award of Distinction
- **Relevant Coursework:** Compilers, Computer Architecture, Real-Time Operating Systems, Digital Hardware, Embedded MCU Systems, Control Systems, Data Structures & Algorithms, UNIX System & Concurrency Programming, Electronic Circuits, OOP